Application No.: 09/588,617 Docket No.: 21806-00083-US

REMARKS

Claims 1-32 remain pending in this application, however, claims 1-7, 11-15, 21, 23-26, and 28-31 are subject to immediate examination in this application, having been elected for continued prosecution. Claim 1 and 30 are independent.

Claims 8-10, 16-20, 22, 27, and 32 were previously withdrawn as being directed to the non-elected species, but have not yet been canceled in light of the potential for rejoinder at the appropriate time. No claims have been amended by this response.

Although no claim amendments have been made by this Response, to aid in the Examiner's review, a copy of the pending claims is provided as an attachment to this Response.

Administrative Oversight in the Official Action

Incorrect Status of Withdrawn Claims

In response to the prior election of species requirement, Applicants previously elected the species covered by Figure 1A, *i.e.*, claims 1-7, 11-15, 21, 23-26, and 28-31 without traverse. Claims 1-5, 13-15, and 30-31 are generic.

In the "Office Action Summary", however, the Examiner incorrectly indicated that claims 8-10, 16-20, and 27-29 had been withdrawn. In addition, the Examiner has apparently rejoined previously withdrawn claim 22, as a substantive art rejection has been made in the pending Official Action.

Claims 28-29 Have not Been Addressed by the Examiner

By Applicants' records, claims 28 and 29 were elected, but the Examiner has not examined or otherwise commented on or rejected these claims in the pending Official Action.

Thus, if a Notice of Allowability is not forthcoming in response to this communication, a new non-final action is requested to clarify the status and make any art rejections of record for all pending claims, as required by the MPEP.

Anticipation Rejection Over Hembree

Withdrawal of the rejection of claims under 35 U.S.C. §102(b) as being anticipated by Hembree (US 6,504,389) is requested.

Applicant notes that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6]

Discussion of Applicants' Disclosure

By way of background, Applicants' disclosure, in one embodiment, is directed to a carrier for test, burn-in, and first-level packaging of semiconductor devices. The disclosed and claimed invention provides, in one aspect, a method for manufacturing and testing semiconductor components that ***combines testing, burning-in and end-use packaging***. In another aspect, a semiconductor structure comprising a device carrier is provided, wherein ***the carrier used for burn-in testing is also used in the end-use application, without removing the device from the carrier***.

The components or semiconductor devices attached to the carrier are tested via interconnect wiring in the carrier. ***The wiring in the carrier is also sufficient for end-use operation of attached semiconductor devices***. The carrier is divided into a plurality of

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[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

components such that each component contains at least one semiconductor device, for example. Those components, including the carrier, are used as the first packaging level of assembly.

By the claimed method and structure, the substantial costs and time associated with initially aligning and attaching chips to the substrate to conduct burn-in, and then removing the chips, separately testing the chip characteristics in a tester, and then reattaching the chips to a final substrate once burn-in and device characterization are completed are avoided by using the burn-in test carrier as part of the end-use package.

Discussion of Hembree

In contrast, Hembree is directed to a test carrier for ***temporarily*** packaging bumped semiconductor components having contact balls. *See* col. 2, lines 19-21. In another embodiment, a cleaning carrier for removing solder contamination from test systems for bumped semiconductor components is disclosed.

Specified Deficiencies of Hembree

In particular, the applied art does not disclose a method for manufacturing and testing semiconductor components, which includes, among other features, "...providing a device carrier, ***said carrier having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices***...and dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device", as recited in previously presented claim 1 (emphasis added).

Further, the applied art does not disclose a semiconductor structure that includes, among other features, "a device carrier...said device carrier having interconnect wiring therein sufficient for both testing and packaging of said semiconductor devices...[and] wherein said carrier is arranged to be divided into a plurality of components, and wherein said plurality of components are arranged so as to be suitably installed in an information handling system without separating said semiconductor devices from said device carrier", as recited in previously presented independent claim 30.

Accordingly, since the applied art does not disclose all the recited features of independent claims 1 and 30, withdrawal of the rejection and allowance of claims 1-31 in this application are respectfully requested.

Conclusion

In view of the above remarks, Applicants believe that each of pending claims 1-31 in this application are in immediate condition for allowance. An early indication of the same would be appreciated.

In the event the Examiner believes that an interview would be helpful in resolving any outstanding issues in this case, the undersigned attorney is available at the telephone number indicated below.

Applicant believes no fee is due with this response. However, if a fee is due, please charge CBLH Deposit Account No. 22-0185, under Order No. 21806-00083-US from which the undersigned is authorized to draw.

Respectfully submitted,

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Enclosure: Listing of the Pending Claims

CURRENTLY PENDING CLAIMS

Although no claim amendments or cancellations have been made by this Response, to aid the Examiner and Applicants in prosecution going forward, this listing of claims identifies the currently pending claims and their status in this application.

CLAIM LISTING:

1. (Previously presented) A method for manufacturing and testing semiconductor components, the method comprising:

providing a plurality of semiconductor devices;

providing a device carrier, said carrier having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices;

attaching said semiconductor devices to said carrier;

testing said devices via said wiring; and

dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device.

2 (Original) The method according to claim 1, further comprising the step of installing one said component on a next level of assembly without separating said device from said carrier.

3. (Original) The method according to claim 1, further comprising the step of installing one said component in an information handling system without separating said device from said carrier.

4. (Original) The method according to claim 1, wherein said carrier comprises a printed circuit board or a flex.

5. (Original) The method according to claim 1, wherein each of said semiconductor devices comprises a plurality of leads and wherein said carrier comprises contacts for external connection, the method further comprising the step of providing a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said carrier contacts.

6. (Original) The method according to claim 5, wherein said lead reduction mechanism comprises a built-in self-test engine.

7. (Original) The method according to claim 6, wherein each semiconductor device comprises one said built-in self-test engine.

8. (Withdrawn) The method according to claim 7, wherein said built-in self-test engine includes less than ten external contacts for controlling said test engine, and wherein said semiconductor devices are connected in parallel to said external contacts for test or burn-in.

9. (Withdrawn) The method according to claim 7, wherein said semiconductor devices are organized in a plurality of groups on said carrier wherein BIST pads on said devices in each group are connected in parallel to separate external contacts.

10. (Withdrawn) The method according to claim 9, further comprising the step of burning-in or testing groups of devices in parallel with a separate BIST reader for each group.

11. (Original) The method according to claim 6, further comprising the step of testing or burning in said semiconductor devices using said built-in test engine.

12. (Original) The method according to claim 11, further comprising the step of separating said built-in self test engine from said carrier.

13. (Original) The method according to claim 1, wherein said testing step comprises running said semiconductor devices simultaneously and independently of each other.

14. (Original) The method according to claim 1, wherein said lead reduction mechanism comprises connecting like leads of said plurality of semiconductor devices in common.

15. (Original) The method according to claim 1, wherein the method comprises dividing said carrier into separate multi-chip final assemblies.

16. (Withdrawn) The method according to claim 15, wherein said multi-chip assemblies comprises single-in-line multi-chip modules or dual-in-line multi-chip modules.

17. (Withdrawn) The method according to claim 1, further comprising the step of

mounting said semiconductor component on a second carrier.

18. (Withdrawn) The method according to claim 17, wherein said carrier comprises a flex, and wherein said second carrier comprises a printed circuit board, a second flex, a ceramic substrate, or a semiconductor substrate.

19. (Withdrawn) The method according to claim 18, wherein said flex comprises leads, said method further comprising separating adjacent leads from each other to facilitate connection to said second carrier.

20. (Withdrawn) The method according to claim 18, wherein a plurality of said components are connected to said second carrier to form an interconnected stack.

21. (Original) The method according to claim 1, wherein said carrier comprises connectors for connecting semiconductor devices on two sides of said carrier.

22. (Withdrawn) The method according to claim 1, further comprising the step of encapsulating said semiconductor devices and said carrier in an encapsulant.

23. (Original) The method according to claim 1, further comprising the step of identifying defective semiconductor devices.

24. (Original) The method according to claim 23, further comprising the step of

invoking redundancy to repair said defective devices.

25. (Original) The method according to claim 23, further comprising the step of removing and replacing said defective semiconductor devices with replacement semiconductor devices.

26. (Original) The method according to claim 25, further comprising the step of repeating said testing, identifying, and removing and replacing until no defective semiconductor devices are identified.

27. (Withdrawn) The method according to claim 25, wherein said replacement semiconductor devices have passed testing and burning-in on another carrier so no further burning-in is required.

28. (Original) The method according to claim 1, wherein said semiconductor devices are memory chips, the method further comprising testing said memory chips at speed.

29. (Original) The method according to claim 1, wherein said testing comprises testing functionality, testing for sensitivities, or testing fuses.

30. (Previously presented) A semiconductor structure comprising:

a device carrier; and

a plurality of semiconductor devices mounted to said device carrier,

said device carrier having interconnect wiring therein sufficient for both testing and packaging of said semiconductor devices;

wherein said semiconductor devices on said carrier are arranged to be tested and burned-in,

wherein said carrier is arranged to be divided into a plurality of components, and

wherein said plurality of components are arranged so as to be suitably installed in an information handling system without separating said semiconductor devices from said device carrier.

31. (Original) The semiconductor structure of claim 30 wherein said carrier comprises contacts for external connection, said structure further comprising a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said contacts of said carrier.

32. (Withdrawn) A semiconductor structure comprising:

a stack of flex device carriers, at least one semiconductor device mounted to each said flex carrier; and

an interconnect substrate, wherein said flex device carriers are electrically connected to said interconnect substrate,

wherein said stack of flex device carriers, said at least one semiconductor device, and said interconnect substrate are interconnected and arranged in a manner suitable for both operational testing and packaging of the semiconductor structure.